

A cross-sectional view of a semiconductor device. The device consists of a **Thin Silicon** layer (12) on top of a **Buried Oxide** layer (11). The **Thin Silicon** layer is divided into a central rectangular region (18) and two side regions (26S). The central region (18) is further divided into a top layer (21) and a bottom layer (22). The side regions (26S) are also divided into a top layer (26P) and a bottom layer (26S). The bottom layer (26S) is shown with a hatched pattern. The **Buried Oxide** layer (11) is shown with a cross-hatched pattern. The entire device is labeled 10.

FIG. 2A

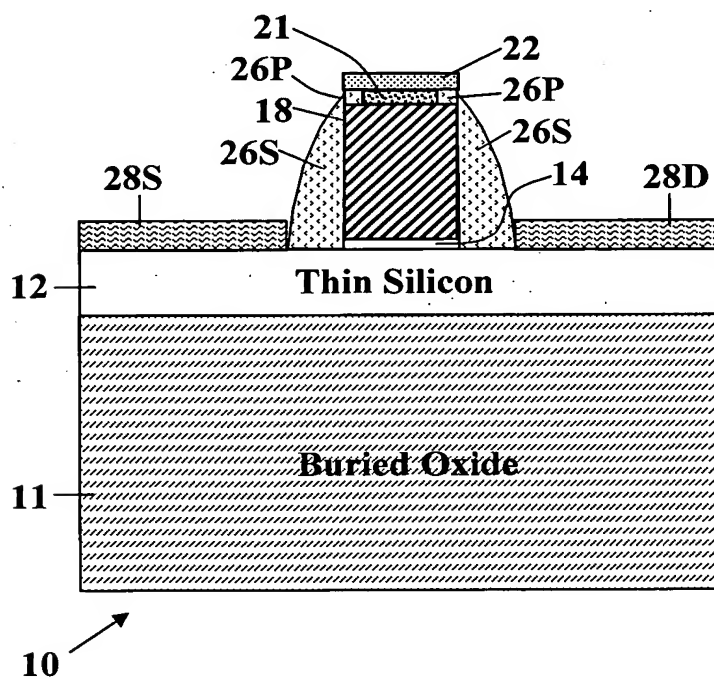


FIG. 2B

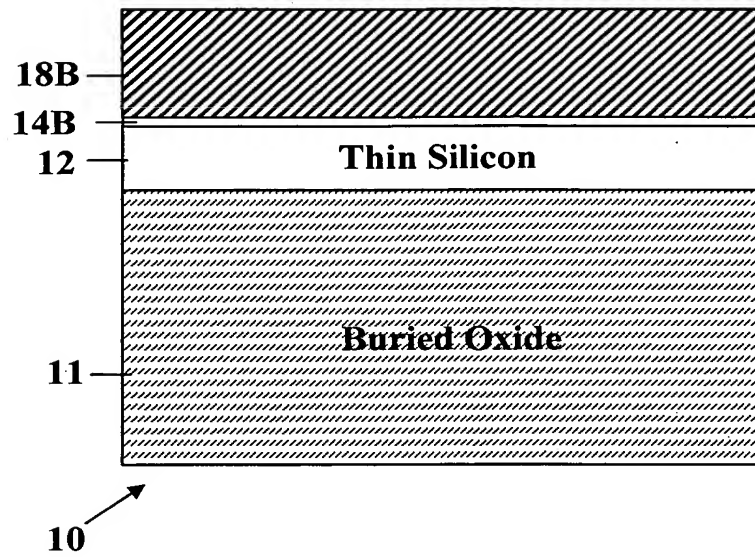


FIG. 3A

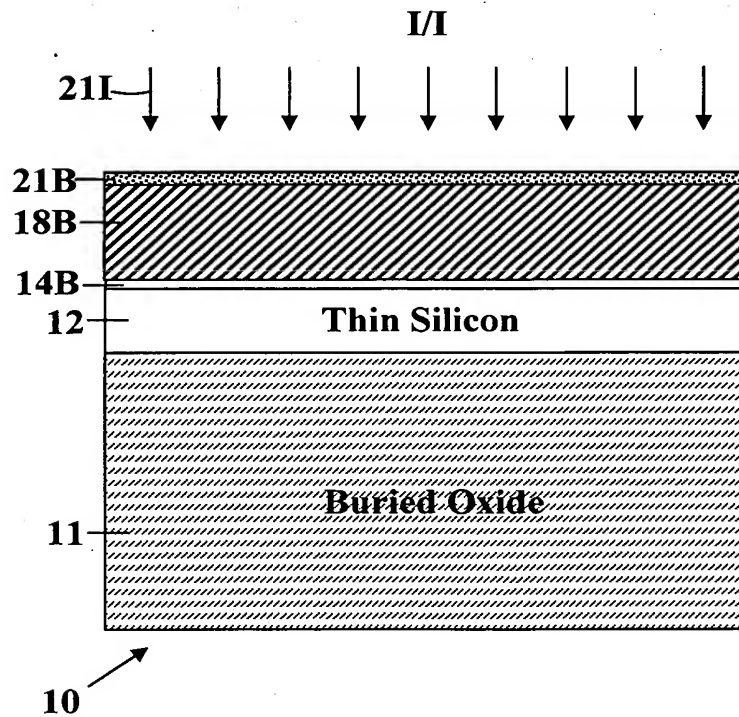


FIG. 3B

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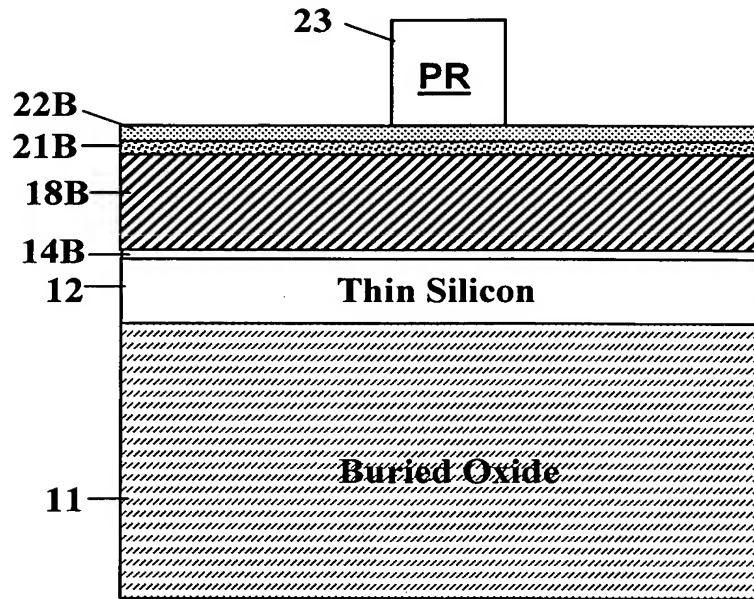


FIG. 3C

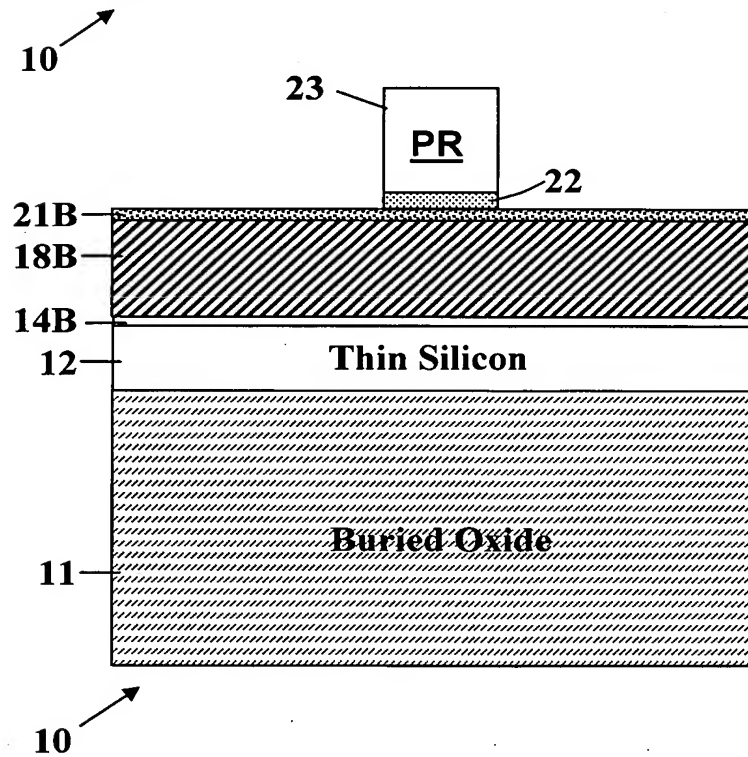


FIG. 3D

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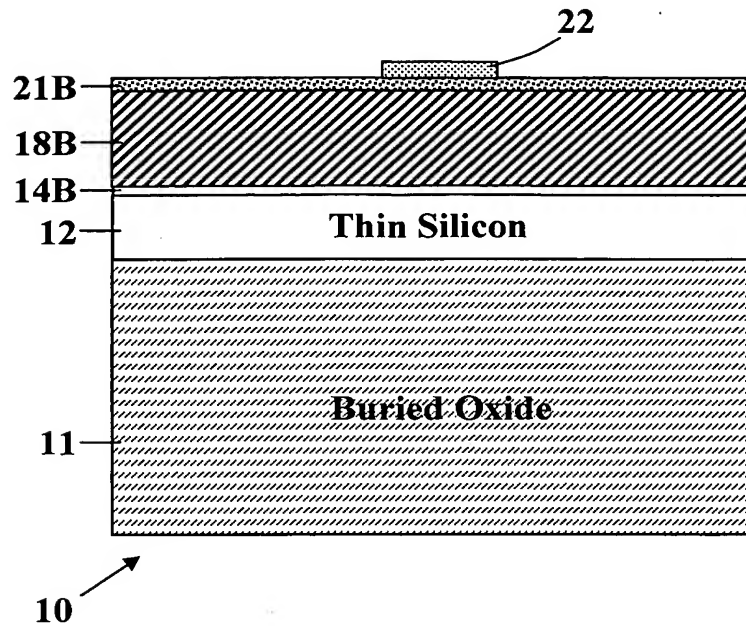


FIG. 3E

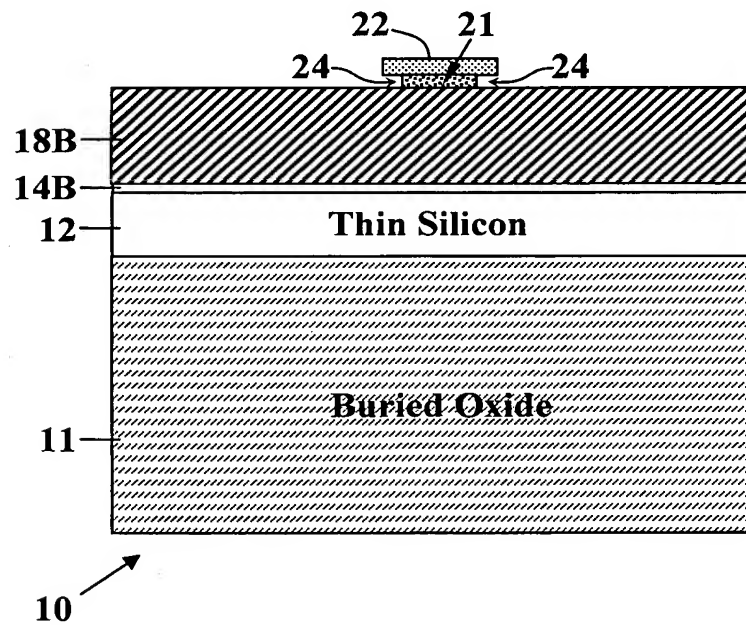


FIG. 3F

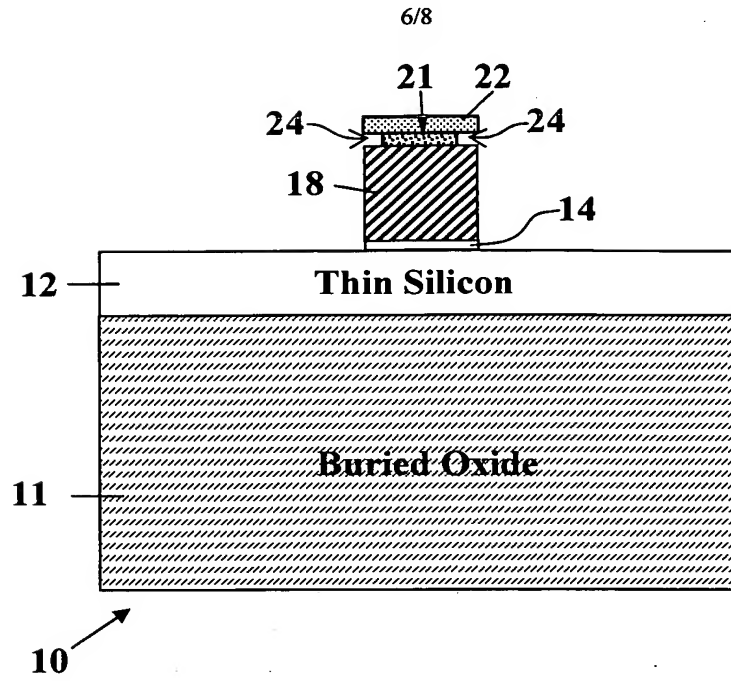


FIG. 3G

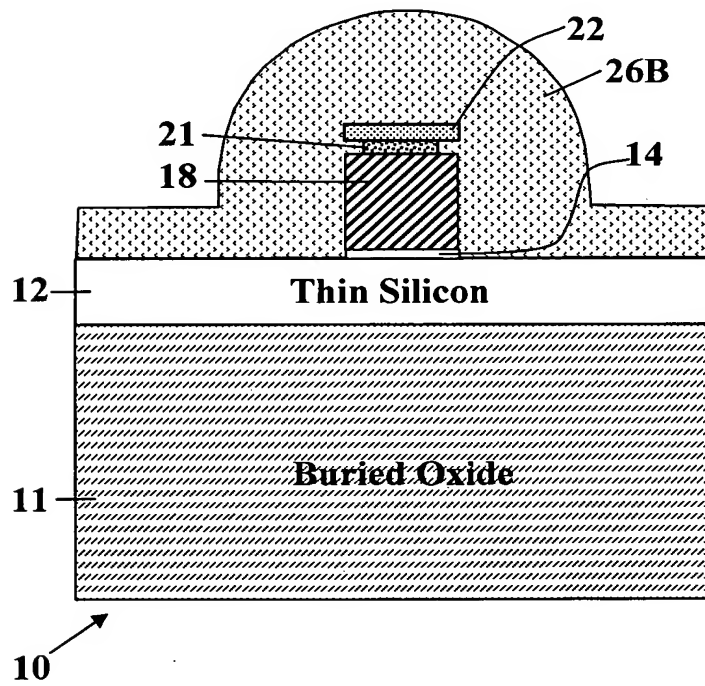


FIG. 3H

FIG. 3I

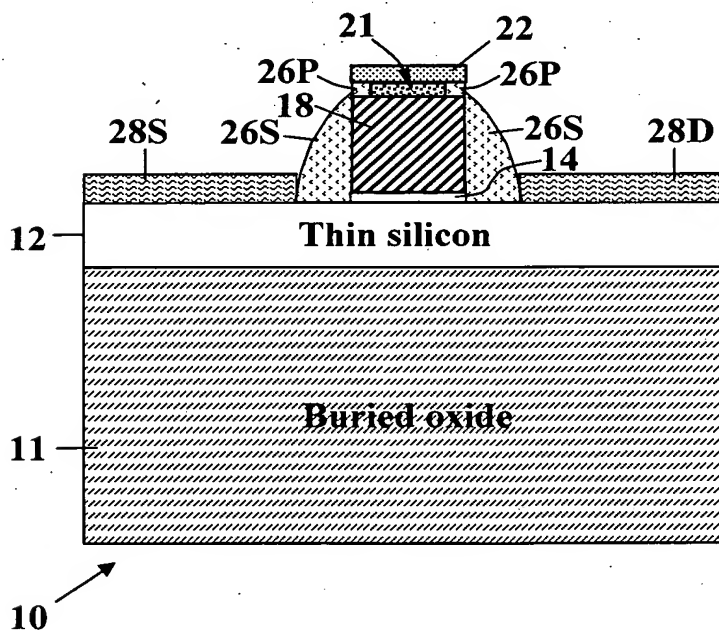


FIG. 3J

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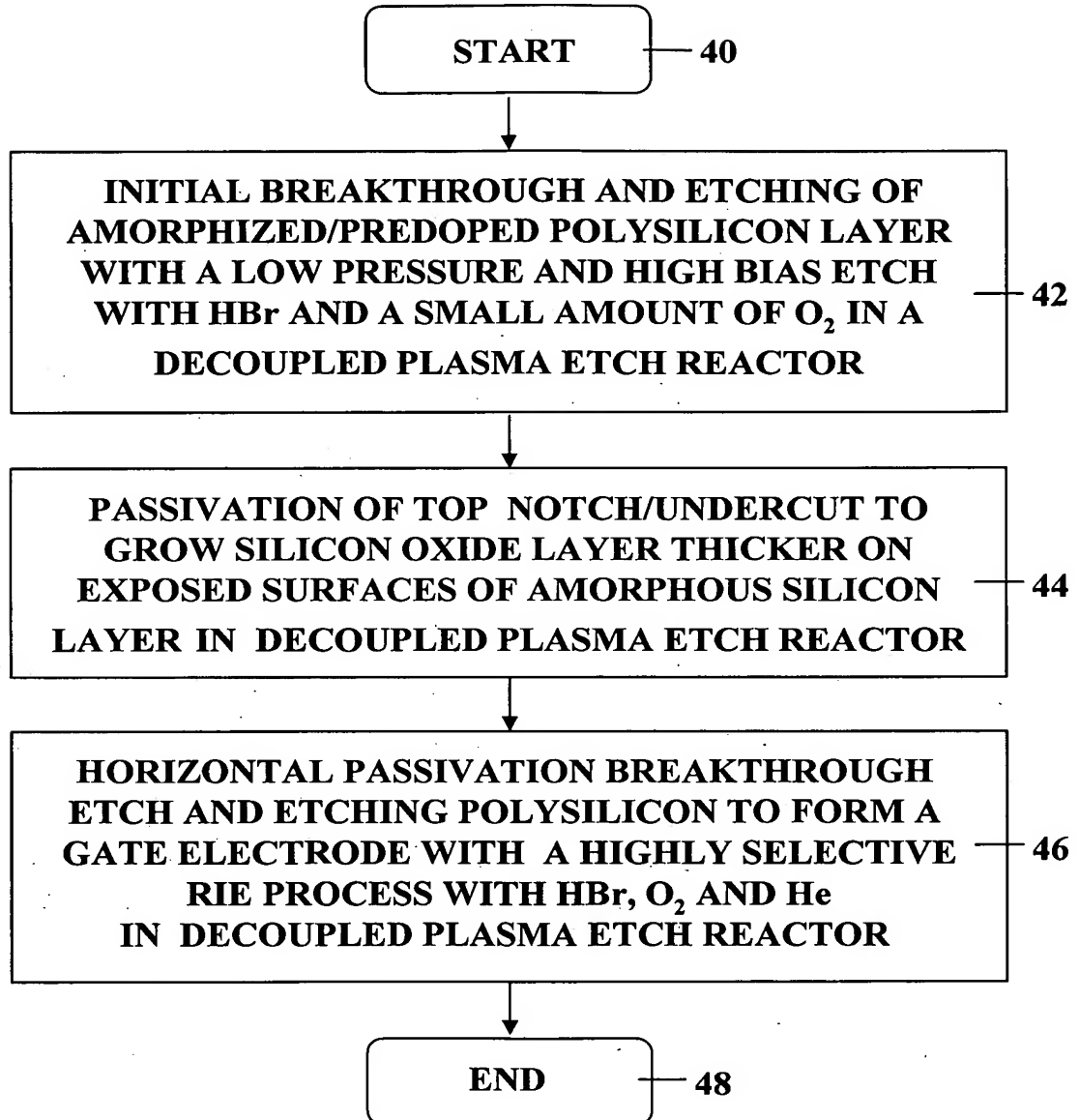


FIG. 4